

ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW
ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

Structures and methods for programmable array type logic and/or memory devices with asymmetrical low tunnel barrier intergate insulators are provided. The programmable array type logic and/or memory devices include non-volatile memory which has a first source/drain region and a second source/drain region separated by a channel region in a substrate. A floating gate opposing the channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator formed by atomic layer deposition. The asymmetrical low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of Al_2O_3 , Ta_2O_5 , TiO_2 , ZrO_2 , Nb_2O_5 , $\text{SrBi}_2\text{Ta}_2\text{O}_3$, SrTiO_3 , PbTiO_3 , and PbZrO_3 .

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